TU Clausthal

Bachelor-, Master- und Doktorandenseminar
des Instituts für Informatik

Construction and Simulation of High-Efficiency Network-on-Chip with Self-Routing Capability

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In order to design a high-efficiency Network-on-Chip (NoC), a simple general classification of inter-processor communication networks and their routing properties are introduced and discussed about being used as a NoC. This thesis proposes a NoC design based on a log2N-network topology, in which each switch is configured by a one-flit input buffer. A range of simulation experiments were implemented. The implementation records help us to explore the relationship between the message latency, the size of a baseline network, and different packet injection rates. Furthermore, they reveal the effect of the message size on the latency of message distributions. Consequently, we comprehend the performance of the proposed NoC explicitly. The proposed NoC can provide low latency for inter-processor communication and be used for real-time applications in multi-processor System-on-Chip (MPSoC).

Mittwoch, den 28.10.2015, 9 Uhr s.t. im
Besprechungsraum 106, IfI, Julius-Albert-Straße 4

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