Control of a Tokamak Fusion Experiment by a Set of MULTITOP Parallel Computers

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Abstract

This papers gives an overview of the parallel computers developped for the fast control system of the tokamak ASDEX-Upgrade. The system consists of six transputer based computers with fixed or variable processor topology. Up to 29 transputers per computer are used together with a transputer control bus and a 'fifth' link concept to fully utilize the benefits of parallel processing using only two types of boards as building blocks.

I. INTRODUCTION

The tokamak experiment ASDEX-Upgrade is Germany's largest fusion facility. Due to the high demands for personnel and machine safety not a single centralized control, but a multi computer, multi processor system was chosen for the tokamak control [0]. Therefore, fatal errors in the case of defects of a single centralized control can be avoided. Together with redundant computers and pure hardware controlled interlocks a slow degradation of the fast multiprocessor system in the case of incidents is to be expected.

Within the complex control system of this experiment six real time computers are of overriding importance for the controlled running of the reactor. Two of them, together with their backups, are responsible for the fast feed forward control of the technical and diagnostical systems of the tokamak and for the fast feed back control of the plasma. Two others are for monitoring overload conditions in the reactor vessel and the magnetic coils.

Common feature of the parallel computers is the MULTITOP architecture [1], which is based on a variable or fixed interconnection network, a topology independent transputer control bus (TSB), a set of worker CPU boards (CPU0s) with 4 Transputers [2] each and some control transputer boards (MCPUs). The boards are VMEbus compatible. The I/O is done via glassfiber links with 10 MBits/s transmission speed. Each computer has a VMEbus based UNIX workstation as a file server and for the graphical user interface. Transputers were chosen as processors, because of their superior price performance ratio in multiprocessor environments and their easy system integration. Furthermore all data from sensors and to actuators are transmitted on serial links, which are directly compatible to the transputer links.

II. THE FEED FORWARD CONTROL

The feed forward control computer has to guarantee a reaction time of less than 10 ms. This includes acquiring and processing of about 100 tokamak signals and a subsequent determination of the tokamak status. For the controlled operation ot he technical subsystems of the tokamak a signalling system is provided called 'timer system'. It initiates locally defined actions at the subsystems. The control of this timer system is done by a 'central timer', which is an integral part of the feed forward computer. Therefore, this computer also has to take care of broadcasting timer and other feed forward signals on a event driven basis.

These demands were fullfilled by a parallel computer consisting of 29 transputers. In fig. 1 the feed forward computer is depicted. It contains (from top to bottom) power supplies, CPU0s with optical converter boards, UNIX host with MCPUs disk and fans.

In fig. 2 we see the block diagram with 16 data collectors, 8 data dispensers, an input- and output master, a central timer, an IOP and a transputer- and VMEbus host. 16 data collector transputers form an input star of 64 links to supervise the tokamak signals. 8 data dispenser transputers realize an output star of 32 links for outputting time- and event dependent functions (trajectories). And 5 transputers (IM, OM, IOP CT, THOST) build the core of control processors for coordinating communication and computation.

The data collector transputers are responsible for inputting, demultiplexing and preprocessing about 100 tokamak signals. After preprocessing most of the signals are condensed into one or two evaluation bits each. The input master transputer then assembles all evaluation bits into an bit vector for the transputer host. The transputer host uses the bit vector as tokamak status information and decides, what the next step is. The data dispensers are responible for outputting values of time dependent functions at the 'right time'. The

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central timer is the signalling instrument for the whole fast control of ASDEX-Upgrade. And the IOP takes care of inter computer comunication.

The feed forward computer is composed by only two types of boards: the CPU0 and the MCPU. In fig. 3 the CPU0 and MCPU board types are shown. All data collectors and data dispensers are realized with CPU0s, which contain 4 separate collector- or dispenser modules. All other functions are implemented by MCPU boards.

A key feature is the scaleable I/O architecture, so that the number of input/output channels can match the requirements. This is performed by a modular 'plug in' concept. The modularity is realized by two means: Firstly the I/O crate is organized in triples called 'triple slots'. This means, that every CPU0 board comes with two optical converter boards, so that I/O and computing is combined. Secondly a new triple can simply added, because of the pluggable transputer control bus (TSB) and input master connections. The TSB is used for booting and syncing of the new board, which is inserted into the chain topology of all transputer boards. After booting, a TSB signal switches the chain topology to the user topology, which is an input star or whatever. Therefore the TSB works in a topology independent way.

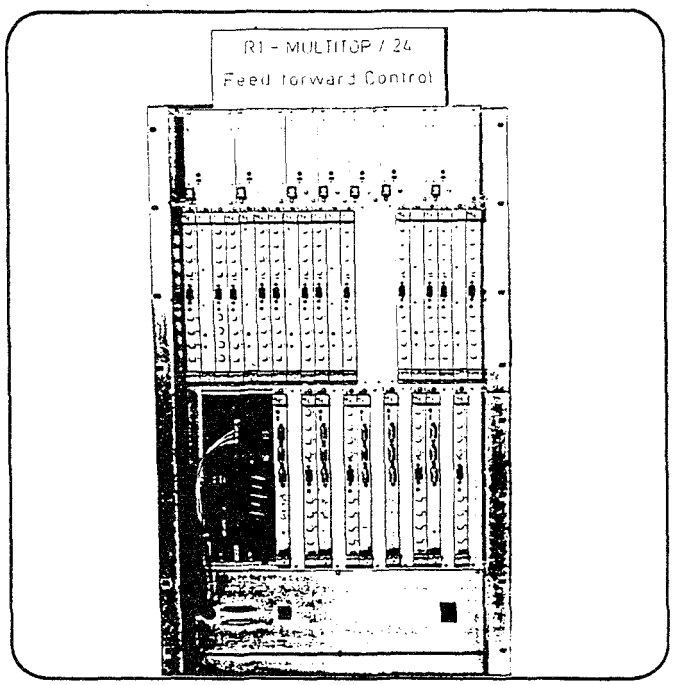


Fig. 1: The view of the feed forward computer, with power supply crate, optical IO channels with CPU0s, MCPUs, disk and fan crate (from top to bottom).

Another feature is the fifth link every transputer memory module has. The fifth link consists of an INMOS linkadapter chip [2]. One or more linkadapter chips can be connected to a transputer bus, so that they are software accessible.

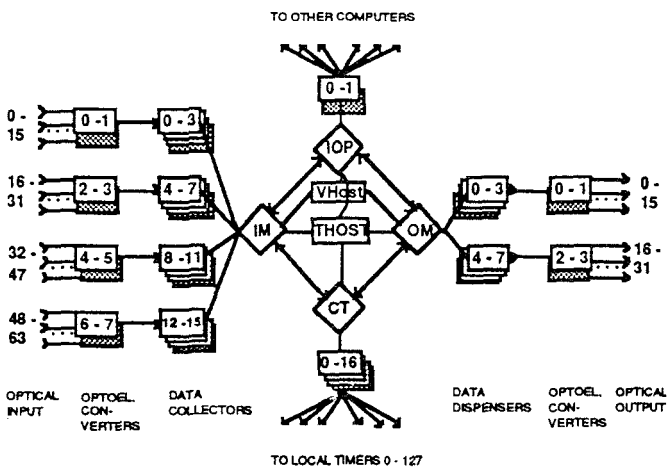
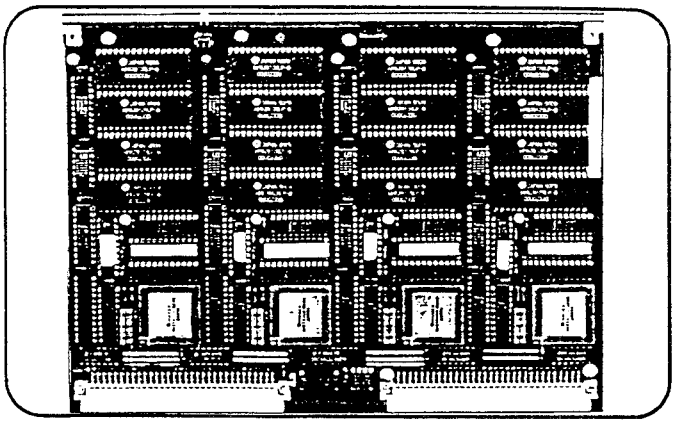


Fig. 2: Block diagram of the feed forward computer. Shown are the transputer- and VMEbus host (THOST, VHOST), input and output master (IM, OM), IOP and central timer (CT), together with the data-collectors and dispensers. More than four links per transputer are made of linkadapters.

The data written to a linkadapter is converted to a link message by the chip. Such an extra link allows for more configurations, more system and debug control, because a set of fifth links can be connected to a Master CPU. 16 fifth links on the MCPU board serve as counterparts to the fifth links on the CPU0 boards. The master can sync and debug the CPU slaves by means of a broadcast and interrupts, which are implemented in hardware on the MCPU. And vice versa, the slaves can access disc and screen via the fifth links and the MCPU, which is normally connected to a VMEbus host. The slow transmission speed of a linkadapter is not a disadvantage for the above applications, because no high data streams have to be transported. Besides its 16 fifth links and the host interface the MCPU board contains 4 MBytes of DRAM and 1 T800 transputer on a double Euro VME card. The CPU0 board has four transputer memory modules with 0.5 - 2 Mbytes fast SRAM each and the TSB interface. In figs. 4 and 5 we see the block diagram of the MCPU and CPU0 boards.

All conversions from optical to electrical signals and vice versa are performed on only one type of board: It has 8 ports with a transmission speed of up to 20 MBits/s per port. It can be jumpered as transmitter, receiver, bidirectional or broadcast. Used as a transmitter the board generates an 'auto acknowledge' for the bidirectional transputer links. A photo of the board is shown in fig. 6.



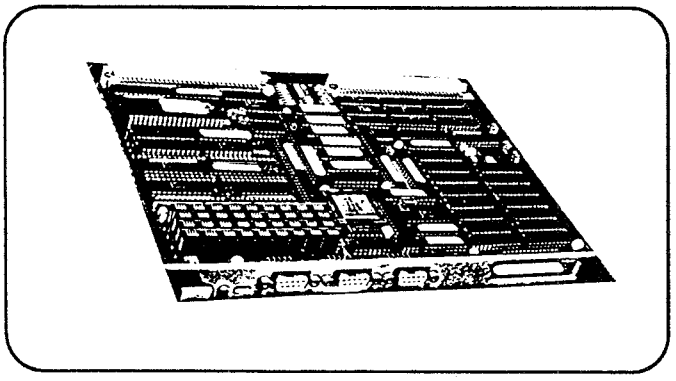


Fig. 3: View of CPU0 and MCPU board (bottom).

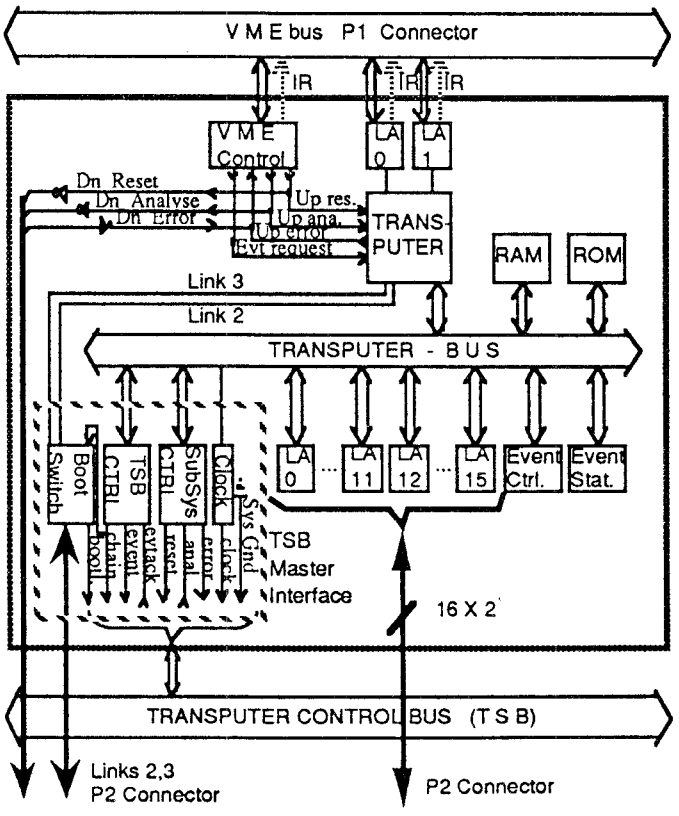


Fig. 4: Block diagram of the MCPU board. LA = fifth link.

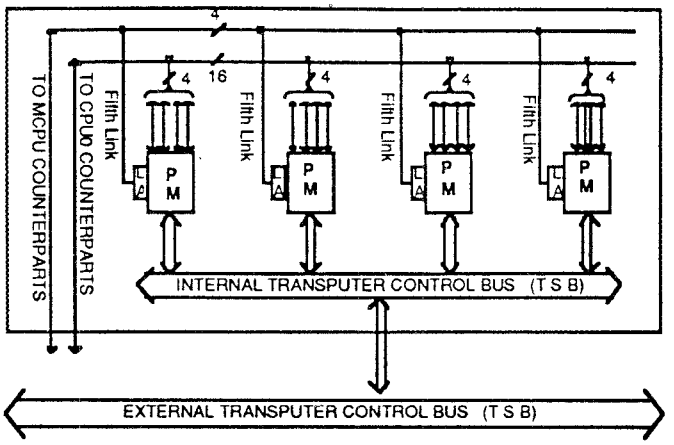


Fig. 5: Block diagram of the CPU0 board. (LA = linkadapter, PM = transputer-memory module).

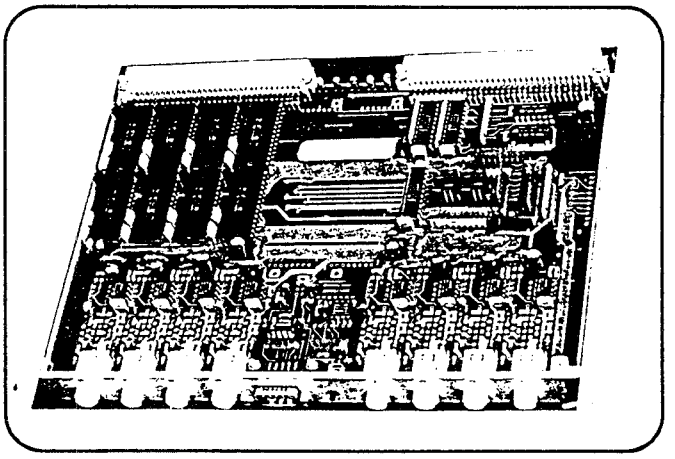


Fig. 6: View of a optical/electrical converter board.

The whole feed forward computer is connected by two special backplanes, one for the triple slot I/O, and one for the MCPUs. The backplanes are in 9 layer stripline technique, to minimize cross talk between the transmission lines and ground bouncing between the power pins. The backplanes contain no active component.

All data from the tokamak is collected online from the sensors via glassfibers. The protocol between sensors, actuators and the feed forward computer is identical with that on the ransputer links, with the exeption, that it is unidirectional. Input data is collected simultaneously from all sensors by means of a central trigger.

The software for the system has more than 10 Mbytes of occam source and a few Mbytes of C for the occam server on the UNIX host. As software development tool the INMOS Toolset [3] was used, which has been ported to the UNIX host system. Because of the fact, that every transputer has its own local software portion, testing and maintenance could be

performed without additional CASE tools. To test the software of the feed forward computer in real time a 'tokamak simulator' has been built. The simulator is in fact a variant of a second feed forward computer, which outputs data in real time, while the first the first feed forward computer puts them in.

III. THE FEED BACK CONTROL

The feed back control computer has to have a deterministic reaction time of less than 1.7 ms. During its cycle time it must take care of input about 50 signals, compute a complex algorithm of about 10 K floating point operations, which are non uniformly distributed, and output 9 signals to control plasma position and shape.

The computer was realized by using 12 computational and two control transputers (3 CPU0s and 2 MCPUs) together with a variable interconnection network. The interconnection network is switched over 3 times every cycle to subsequently form the input, a torus and and the output topology. This is the key feature of the feed back control computer. It allows for both: massively parallel I/O with the I/O topology and application matching with the torus topology. Therefore the interprocessor communication can be minimized and the efficiency kept high. During the input phase of the software cycle 48 transputer links are switched to the optical input converter boards, so that the total input bandwitdh sums up to 50 - 60 MBytes/s. After the data is read in from the sensors and processed, 9 links are switched to optical output converters. The torus computing topology, which is related to the well known hypercube topology, has proven valuable for the application software.

A photo of the feed back computer is shown in fig. 7. The block diagram from an architectural point of view can be seen in fig. 8. The user is more concerned with the application topology shown in fig. 9. The backplane of the feed back computer is a special development in 9 layer stripline technique with an integrated interconnection network. The network is made of 4 standard INMOS link switch chips [2], but because of the limited space on the backplane the net is mechanically built up three dimensionally. The damping resistors for the transputer links are integrated in a mechanical entity called 'damping cube'. Four such damping cubes are mounted between the link switches and their sockets on the backplane. This unconventional setup was necessary to meet the mechanical and electrical constraints. The layout of the backplane is highly optimized for correct signal transmission without any ground shift or cross talk. This is a key prerequisit.

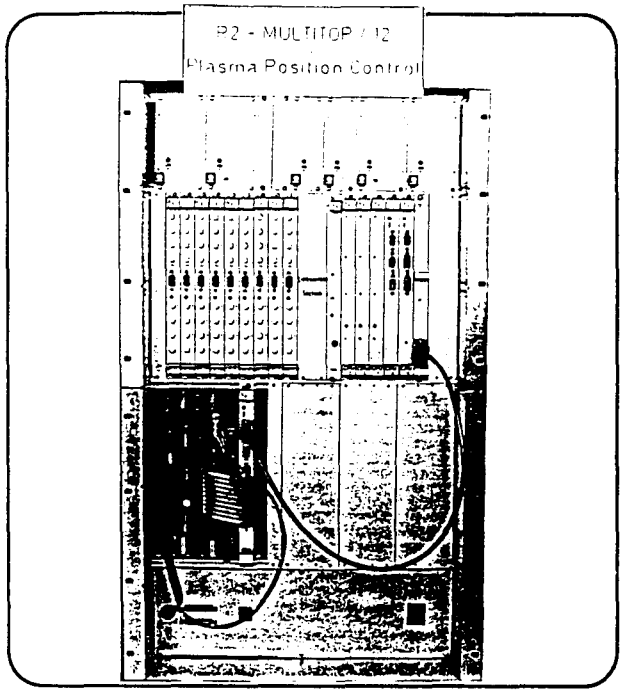


Fig. 7: Photo of the feed back computer.

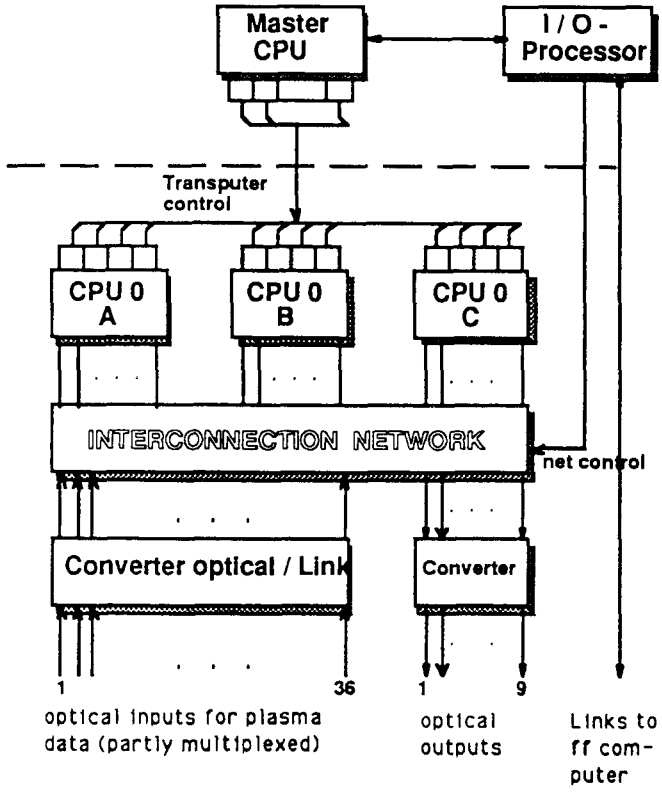


Fig. 8: Architectural block diagram of the feed back computer.

The periphery of the feed back computer is unidirectional'y connected with the computer via glass fibers. The transputer link hardware is used as transmission technique combined with auto acknowledge (transmitting) respective no acknowledge (receiving). All data is sampled at the same time, initiated by a common trigger.

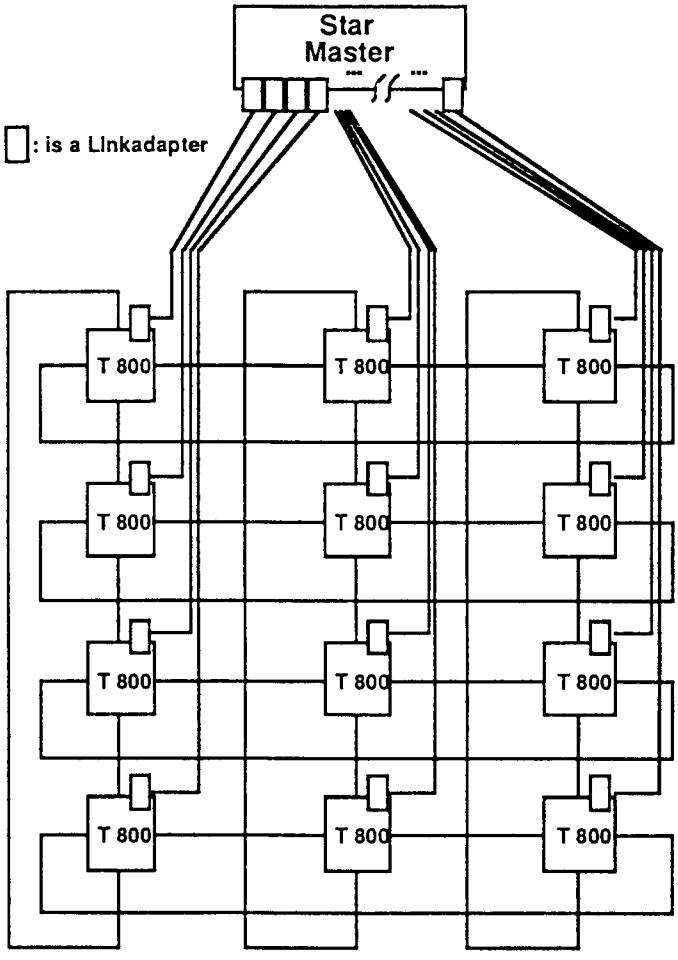


Fig. 9: The Programmers point of view of the feed back computer is a torus with superimposed star topology.

The software for the feed back computer was first written in FORTRAN [4] on a conventional computer to test the algorithm for the plasma position control [5] and afterwards parallelized and ported to occam [6]. As software development tool the Inmos TDS [7] is used, which has been adapted to the UNIX host system. The occam code is tuned to match the strong time requirements of 1.7 ms cycle time. For the final system integration the feed forward computer was necessary, because it controls the running of the feed back computer. Not to delay the first operation of the feed back computer, a little simulator of the feed forward computer was installed, which initiated the control commands the feed back computer needed.

To increase the reliability of the plasma control, a backup system of the feed back computer is run in parallel. It inputs the same input data as the main feed back system, but it outputs data only to the feed forward computer, which compares the two sets of data 'on the fly'. If they don't match, an emergency stop is initiated. So, only the output of the main feed back system is connected with the actuators.

Both computers, feed forward and feed back, have local area network ports to other realtime computers, technical and diagnostical subsystems and the IPP computing center. The CPU0 and MCPU boards, the backplanes and the optical converters are special developments, which are potential building blocks for a whole range of parallel computers.

IV. VESSEL AND COIL MONITORING

Two MULTITOP computers are dedicated to monitor approximately 400 tokamak signals, which give information about the mechanical forces in the vacuum vessel and the coils of the reactor. They have to detect any overload condition. In fig. 10 a block diagram is shown. The computers have 5 transputers each (1 MCPU and 1 CPU0), and their input signals are multiplexed onto four links. Their time scale is 50 ms, which is sufficient for monitoring mechanical forces. Both computers are transputer linked with the feed forward computer and the sensors via glassfibers. The same backplane as in the feed forward computer could be used.

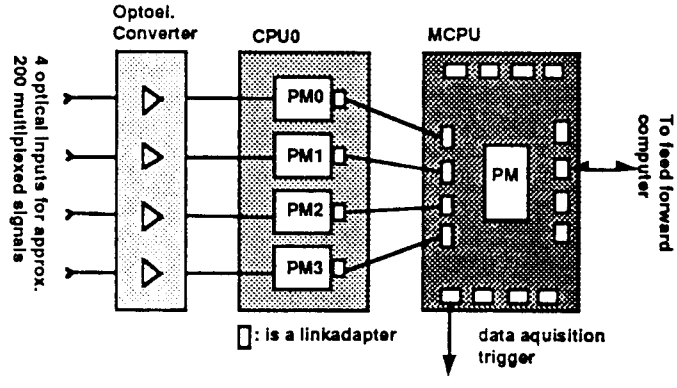


Fig. 10: Block diagram of one monitor computer.

The monitor computers are interesting from a software point of view. Because the application program is coded in transputer FORTRAN and is linked together with occam and C system subroutines into one executable image. Occam is

used for all real time I/O, while the FORTRAN code contains the main control loop and the numerical algorithms [8]. On the UNIX side standard C code is used for the server of the transputer programs.

V. RESULTS

The fast control of ASDEX-Upgrade has gone into operation and it has proven working reliably. The plasma is feed forward and feed back controlled in the desired cycle time. The technical and diagnostical systems are supervised and a comfortable fusion management with online reaction has been established. So the MULTITOP computers have met the requirements. The transputer control bus, the fifth links, the variable interconnection network and the modular and hierarchical structure have proven valuable hardware support for the software. The last fact, which speaks for itself, is, that all time schedules could be held, despite the new parallel processing technique used. Also costs have been relativly moderate.

VI. ADDITIONAL INFORMATION

The Annual Reports 1989 and 1990 of the Max-Planck-Institut für Plasmaphysik contain a comprehensive description of the whole control of ASDEX-Upgrade, which was a collaborative work of the divisions of 'Experimentelle Plasmaphysik 1', 'Informatik' and 'Theorie 3'.

VII. REFERENCES

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