The Timing System for the ASDEX Upgrade Experiment Control

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Abstract

For the adaptive control system of the ASDEX Upgrade tokamak experiment a new digital timing system was developed. Its structure is centralized and distributed. The timing system defines a systemwide 100 nanosecond absolute timescale by central generation of clock and time zero information. Distributed processes are synchronized by time events and state events generated centrally. The timing system supports preprogrammed operation and as a new feature adaptive operation in close collaboration with the central control computers. A standard modulation technique allows to distribute simultaneously the time and event information via fibre optics cables. The timing system is remote controlled by internal functions using the same fibre optics.

This paper summarizes the ASDEX Upgrade timing system design and implementation, and aspects of the integration into the control system .

I. INTRODUCTION

The operation of large scale experiments is based on the proper synchronization of various distributed technical and diagnostic processes. Timing systems generate and distribute event and time information to coordinate these processes.

Event information is generated in either a preprogrammed or event dependent way. Preprogrammed or timer events are produced by predefined time intervals. Event dependent or state events are generated by a change in the system state, indicated by signals from the machine or the experiment.

In real-time systems time information is used to initiate or execute time dependent processes and to protocol the evolution of processes. Time is measured by counting periodically generated clock pulses. To get comparable absolute times among different counters, common clock and common counter reset as a time zero event are needed.

Contemporary timer systems use two alternative techniques:

Analog timing systems structure is simple and usually based on signal loops. These systems can only handle a limited number of events, because of the limited number of transmission wires. Examples are timing systems using one wire with several active analog dc levels or several wires with one active dc level. An event is indicated by a change in the analog level. The event serves as a synchronization trigger without explicit time information. The total number of events is limited by the number of levels and the number of wires. A more complex example is the JET timing system CTS [1]. It consists of 4 channel node modules. A common input trigger is delayed with a preprogrammed time and produces output triggers. With tree structured fibre optic cable transmission between subsidiary nodes, a distributed system for the generation of chained time pulses can be built. The total number of events is limited by the number of nodes. An additional central 1MHz clock which is distributed separately allows to synchronize local clocks and to measure times by a stopwatch module.

Digital timing systems show a complex structure. They can easily be integrated into modern computer controlled systems and handle a big number of events and offer additional services. An example is the RFX timing system STC [2]. Encoder modules triggered externally generate preprogrammed event codes. The event word is imprinted on a clock carrier and distributed to decoder modules or additional encoder modules via a daisy chained optical highway. The decoders regain the 1MHz carrier for local use. The event code is matched to trigger outputs to local processes as preprogrammed. Time events are chained by hardware feedback connections between decoders and encoders to give the global sequence. The total number of events is limited by the binary word size. Decoders provide various services to control switches and waveform generators and to produce timestamps for events.

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For the ASDEX Upgrade experiment a new digital timing system was designed to control the experiment in close collaboration with a digital control computer system. Special care has to be taken to give improved support of the control system's adaptive mode of operation.

II. GENERAL ASPECTS OF TIMING SYTEM DESIGN

Timing systems interact with time dependent experimental, technical and diagnostic processes by exchange of event and time information. The experimental environment and the structure and dependencies of the participating processes have to be analyzed to match the structure and organization of the timing system to the experimental requirements.

The timing system's basic task is the systemwide synchronization of processes. Some of the processes, e.g. technical processes, will be mandatory to run the machine. Others, e.g. diagnostic processes and control of subdevices, will be useful to run the experiments but not ultimately necessary to guarantee the machine's integrity. Hence, there exist processes of global and of local importance. Processes of global importance are best controlled by a central system to guarantee the proper main sequencing of the machine operation. Local processes should be controlled locally, their sequencing adjustable by local operators, to allow for flexible operation. A universal timing system has to support both the central control of important global processes and the synchronization of optional local processes. The synchronization between central control and the optional processes can be done by state event information. Then, no central knowledge about local actions is needed.

Deterministic systems need no process feedback and can be run in a preprogrammed way by timer events. Such systems have a simple structure and are easy to operate. Nondeterministic systems require process feedback into the control system to allow for reactions. State events then have to be generated by real-time monitoring of process signals. Such systems are more complex but can adapt to the experimental process. In both cases a central event generation device has to produce timer or state event information for the control of global processes. The minimum number of required events is defined by the number of independent parameters needed to coordinate the main sequencing of the global processes.

Time information is needed to execute time dependent processes or to protocol the temporal evolution of processes or events on an absolute timescale. Time information can be produced locally, for selected local processes or centrally, common to all processes. Local time counters using local clocks or local time zero events minimize the efforts to distribute time information. However, they suffer from drift and low accuracy, due to limited quartz precision and undefined time zero event. A central time generator which produces and distributes a central clock and a central time zero event to remote control local time counters offers absolute systemwide time information, but requires additional hardware. The decision about locally or centrally defined time depends on the required time accuracy and comparability.

Real-time control computers always have to be coupled to the central time to guarantee an absolute synchronization between all control processes.

The time resolution or clock frequency is defined by the characteristic time of the shortest technical or physical process which has to be controlled or protocolled. The time range or time counter width is given by the longest time, usually the experiment cycle time.

The event and time information has to be distributed throughout the whole experimental system for the control of peripheral processes. Central filtering of information and subsequent appropriate routing to local devices needs central knowledge about the local use of event information, and adequate central computing power for filtering. Local peripheral filtering of broadcasted information requires local intelligence, but the central system becomes simple. Furthermore, local changes in the use of event information, e.g. processing of additional events, can be done locally. This is a desirable aspect for the operation of a widespread timing system.

III. THE ASDEX UPGRADE ENVIRONMENT

ASDEX Upgrade is a large scale physics experiment of tokamak type. Tokamak machines are at present the most advanced devices to run and examine plasma discharges on the way to a controlled nuclear fusion reactor. Process timescales range from microseconds for changes in the magneto-hydrodynamic plasma behaviour to minutes for the power supplies charge-up and hours for glow discharges or vessel heating. 16 dedicated programmable logic controllers (PLCs) for configuration and slow control and some tens of diagnostics require the precise coordination of some hundred processes to run the experiments. The fast adaptive discharge control is done by a cluster of real-time control computers on a milliseconds timescale [3] .

The ASDEX Upgrade timing system has to collaborate with the central control computers to directly control the global experimental process (fig. 1).

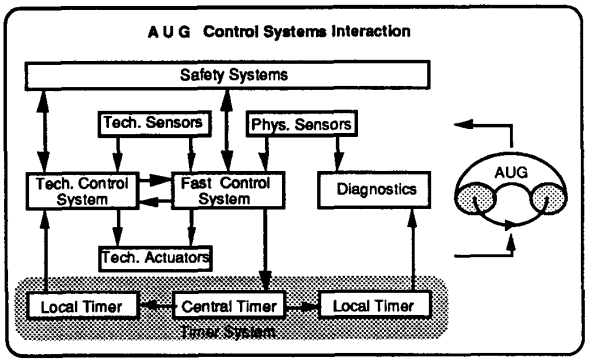

Fig. 1: Structure of the AUG experiment and control system.

Local diagnostic processes may freely join the main sequencing. The ASDEX Upgrade discharge control includes preprogrammed and adaptive operation, both of which have to be supported. Therefore, the timing system uses both timer events and state events. Subdevices which control parts of the experiment are widely distributed, with a central control computer. The timing system has to be centralized and distributed.

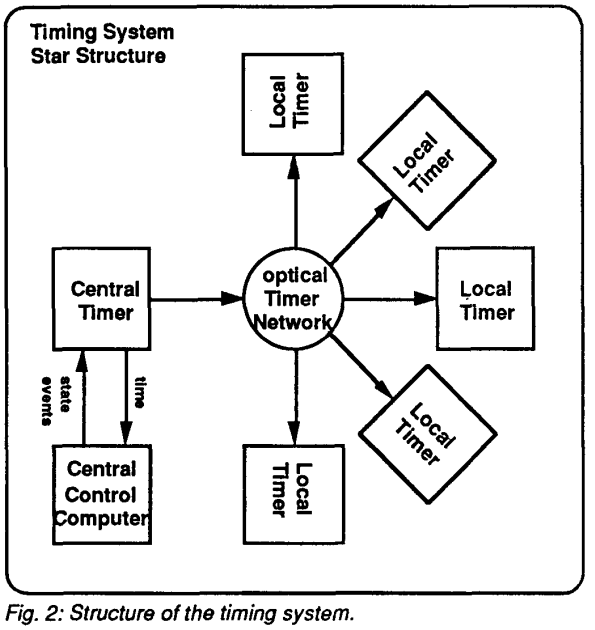

Fig. 2: Structure of the timing system.

A central timer is an integral part of the central control computers. Local timers are distributed throughout the experiment and attached to peripheral devices (fig. 2). About hundred local timers are needed for the experiments final setup. A timer network transfers the information from the central timer to the local timers. Due to electrical boundary conditions, distribution of information has to be done by fibre optics. Simple installation and flexible operation are further demands.

Real-time control processes as well as diagnostic data acquisition for ASDEX Upgrade need an absolute timescale. Thus, central clock and central time zero event and their systemwide distribution are mandatory. The absolute time accuracy should be better than microseconds, with a total range up to many hours.

IV. IMPLEMENTATION OF THE ASDEX UPGRADE TIMING SYSTEM

A. Central Timer

The central timer uses the same hardware as the control computers. It is based on a VME board (fig. 3) with a 32bit RISC type T800 transputer, 4 high speed serial transputer links and 16 additional link adapter parallel ports [4]. The workstation's VME bus can be accessed by one link if jumpered.

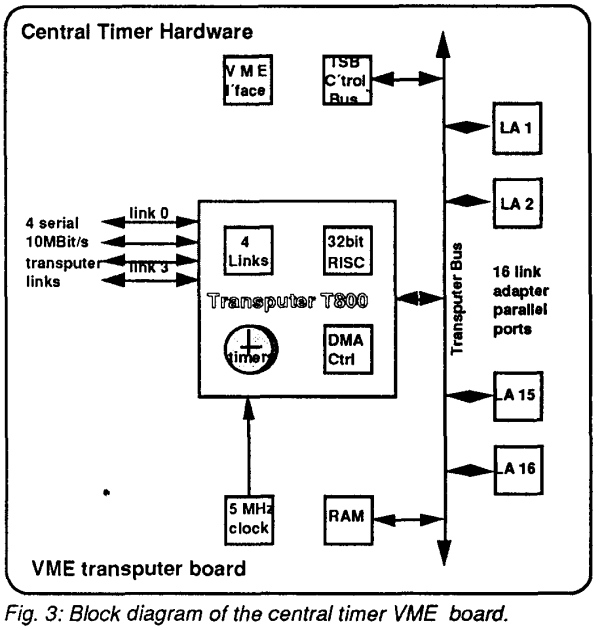

Fig. 3: Block diagram of the central timer VME board.

The preprogrammed time event generation is done by program control. The required configuration parameters to preset the transputer timers are filtered by the central timer from the control computer's downloaded shot program before

shot. Real-time switching between alternate shot programs is included. Event informations from the control computer's monitor processes are passed to the central timer by a serial transputer link. As a future option for a systemwide interlock facility, the 16 parallel link adapter ports will serve for the central timer's private low level process monitoring, producing a small number of interlock events. The central timer's multiplex process combines all the generated timer events, state events and interlock events into one event output stream (fig. 4).

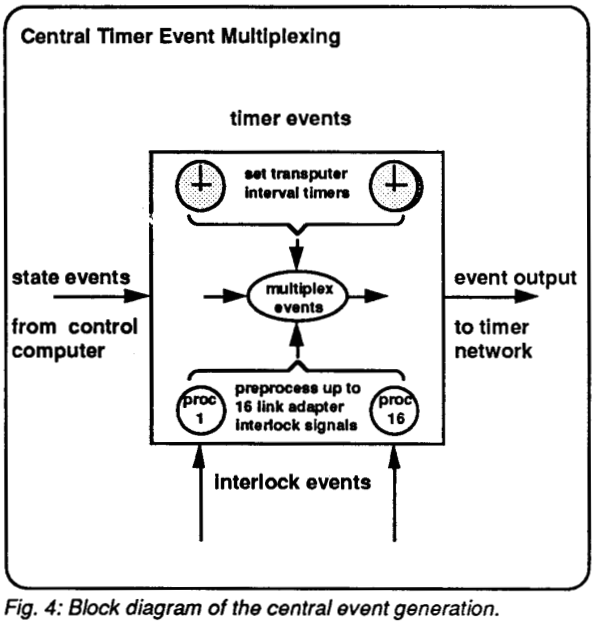

Fig. 4: Block diagram of the central event generation.

The central timer generates the system clock both for the central control computers and for the timing system (fig. 5). Time events are produced by the central timer as defined by the downloaded shot program. The central control computers generate state events by monitoring the experimental processes and pass them to the central timer. The central timer's event and time information is broadcast systemwide via an unidirectional fibre optics star network. Local timers reconstruct the time and event information. The event information is filtered and mapped to trigger outputs to control local processes. The time information may be passed on to local processes. All local timer actions including execution times are protocolled internally.

A 10MHz clock is part of the central timer and serves as system clock. It is distributed to the timer network as well as to the control computer's transputers (clocked down to the required 5MHz). An absolute time zero information is generated during the experiment preparation phase by a synchronization process between the control computer and the central timer, and distributed to the timer network. An additional event dependent time zero is optional (see local timer).

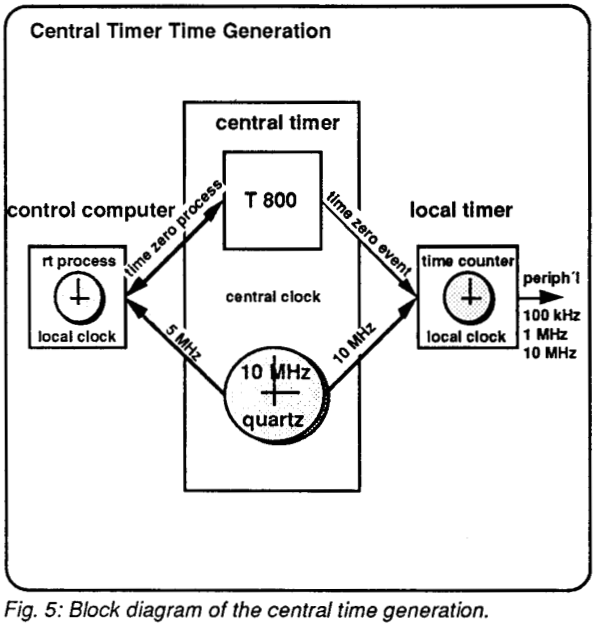

Fig. 5: Block diagram of the central time generation.

B. Timer Network and Transmission Technique

The network's task is the simultaneous distribution of event and time information. The event information is carried by the central timer's asynchronous serial 10MBit/s transputer link output. The clock information is synchronous 10MHz. Both informations are Manchester modulated into a synchronous serial 20MBit/s signal. (fig. 6)

To guarantee a high level of security, 8 bits of redundant 2 bit error detection and 1 bit correction (EDC) information is added to each 32bit timer event before transmission. The distribution of the data stream is done by a unidirectional fibre optics star topology network. It involves electrical multiplication of the central timer output signal and subsequent electrical-to-optical conversion.

As future option, an additional acknowledge ring may be installed. It gives an overall feedback information from all local timers to the central timer and can be jumperd either to positive acknowledge correct data and operation or to negative acknowledge erroneous data or failures. However, the very reliable operation of the timing system doesn't require the addition of an acknowledge ring.

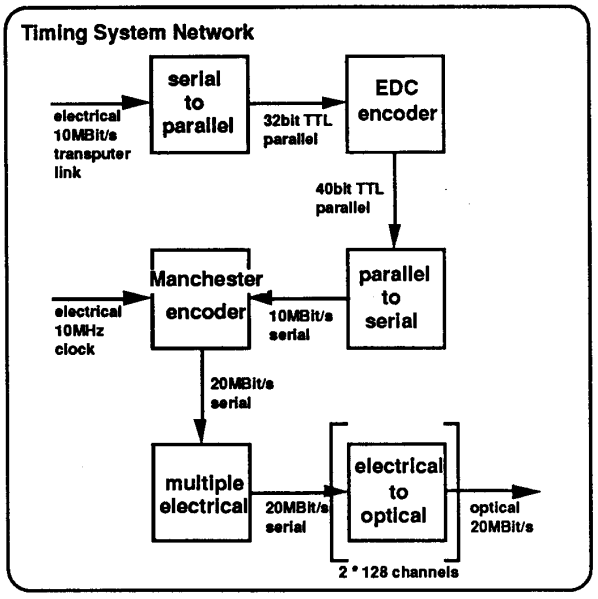

Fig. 6: Block diagram of the the timing networks transmission technique.

C. Local Timer and Modes of Operation

The local timers are low cost dedicated devices, based on standard TTL chips. A local timer module consists of 3 Euro-size boards with plug connectors. A fourth board for protocolling of local processes can be added as an option.

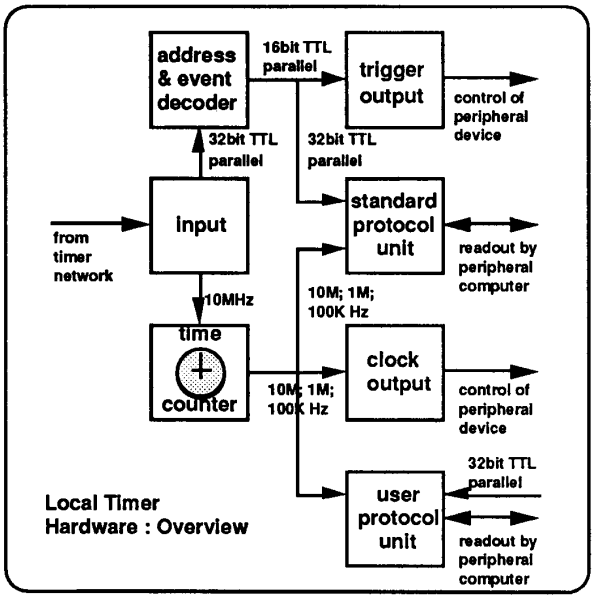

Fig. 7: Overview of local timer module.

The local timer's tasks is to receive, decode and execute the centrally distributed time and event information and to protocol all executed actions. It consists of several functional blocks as depicted (fig. 7).

First, the incoming signal is converted optical-to-electrical. Then, Manchester decoding separates the serial event and time informations (fig. 8).

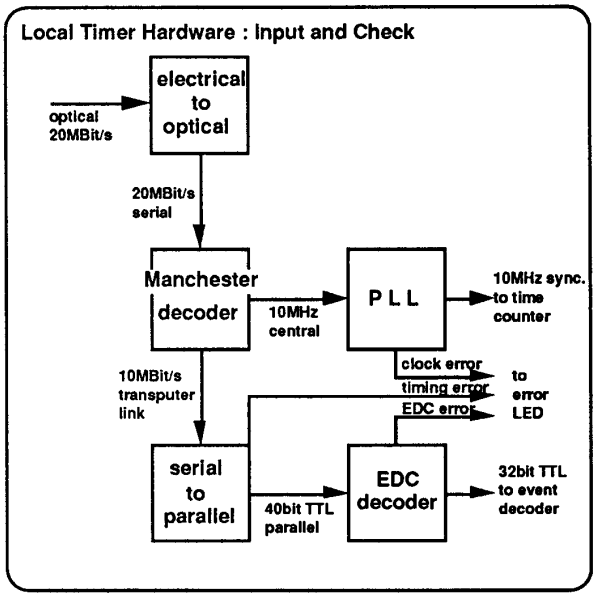

Fig. 8: Block diagram of the local timer input and error checking.

The received 10MHz central clock synchronizes a local 10MHz PLL circuit (fig. 9). In case of a central timer or network failure, the central clock is replaced by a local clock (which gives accurate time for about 10**5 clock cycles). This high level of local fault tolerance against clock failure allows to clock local real-time computers with the central clock. Error states detected by a local timer module are indicated by latched LEDs, some of them being protocolled, and by the acknowledge output. Checks are performed for the correctness of the central 10MHz clock, the timing of the event information and redundant EDC information.

The reconstructed clock can be subdivided in the local timer by adjustable factors of 1, 10, 100 to match local requirements. The clock is used both for external output and for internal counting of the central time by a 32bit time counter. Maximum time resolution is 100 nanoseconds for a total of 6m40s, maximum time range is 11h at 10 microseconds time step.

The systemwide time zero reset is executed by remote control with the help of internal functions. Internal functions are distributed in the same way as event information and

executed by a specific internal function decoder which controls the local timer's operation. Two time zero reset modes are implemented. One is an absolute reset, which resets the time counter before protocolling. This gives the experiment's technical timescale. The other is an event dependent reset, which protocols the actual time and then resets the time counter. Usually, the timing system starts with an absolute reset at the beginning of the technical shot preparation, and can be reset again by a specific event e.g. the ignition of the plasma current. This gives the physical timescale. The relation between both timescales is protocolled. Execution of absolute and event dependent time zero reset can be jumpered on board according to local needs.

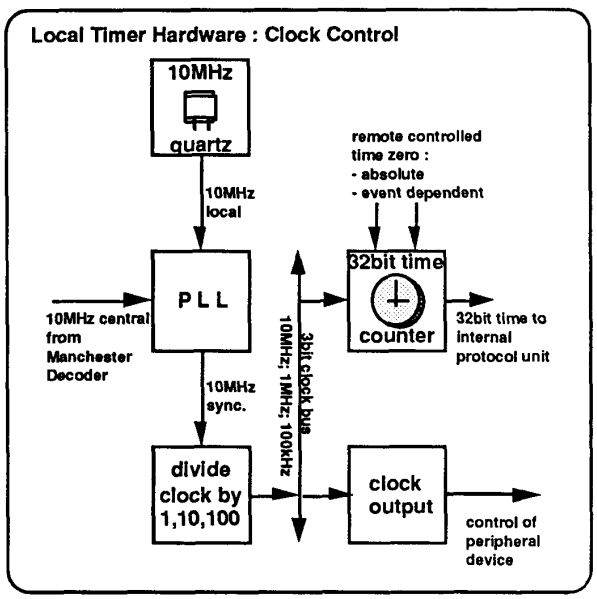

Fig. 9: Block diagram of time reconstruction by local timer.

The 10MBit/s event information is converted serial-to-parallel and EDC decoded. The 32bit event word is then decoded for addressed mode of operation and addressed local timer module (a broadcast address common for all local timer modules is implemented in addition). Only events which are coded correctly are executed by the addressed local timers.

The event information is interpreted, depending on the selected mode of operation (fig. 10). The mode is defined for each transmitted event. There exist four modes.

In event mode, the event number is filtered and mapped to the 8 trigger output channels by local timer tables according to user specification. These tables are EPROM based with a size of 64k event x 16bit output-select. Thus, event dependent control of local processes is supported. Events and related actions have to be defined locally. The EPROM based event filtering and mapping has shown to be easily adjustable to local process requirements. The possibility for event dependent operation of the control system results in a system inherent flexibility to react to real-time events. Static EPROM tables are then sufficient. Thus, dynamic RAM configuration with filtering tables was not implemented, even though it would have been feasible.

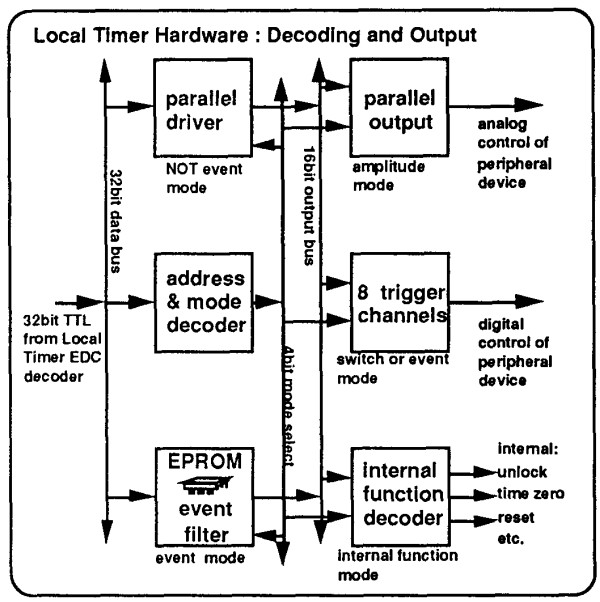

Fig. 10: Block diagram of event decoding and execution.

In switch mode, the 8 trigger output channels can be directly selected and set for preprogrammed switch device control.

In amplitude mode, a 16bit parallel port can directly address peripheral DACs for preprogrammed analog device control.

Internal function mode allows for central remote control of the local timers. Implemented functions are module lock / unlock, time zero reset, module reset, acknowledge mode. Each of the up to 255 local timers can be controlled by internal functions individually, e.g. be locked or unlocked for specific test procedures.

Mode 8bit	Timer Address 8bit	Command Code 16bit
Event	local timer 1-255 or broadcast 0	16bit event number (mapped to switches by EPROM)
Switch	local timer 1-255	8bit trigger channel select mask + 8 bit trigger channel data mask
Amplitude	local timer 1-255	4bit peripheral DAC address + 12 bit DAC amplitude
Internal Function	local timer 1-255 or broadcast 0	4bit internal function number + 12bit function parameters

Table 1: 32bit encoding for the 4 modes of operation.

Event mode and internal function mode may be addressed individually or by broadcast to be executed simultaneously by all local timers. Switch and amplitude mode may be addressed only individually Table 1 gives an overview of the encoding of the different modes of operation.

All executed events including the 32bit event word and 32bit execution time are automatically protocolled by each local timer module. The time counter is remote controlled for time zero reset. Up to 2k events can be stacked. The information can be read out from a local computer by parallel or RS232 ports at any time.

An additional user protocol module can be attached It provides a service for users to protocol private 32bit informations with timestamp on the absolute timescale. The time counter is remote controlled for time zero reset. Up to 2k 32bit messages can be protocolled at a maximum rate of 10 microseconds per message. Readout is the same as for the local timer's standard protocol unit.

V. RESULTS

The ASDEX Upgrade timing system hardware and the Manchester transmission technique were found to be very reliable and safe. High efficiency and performance were achieved by the the simultaneous transfer of time and event information via fibre optics and remote control of the local timers using the same path.

The central control computers and the timing system cooperate closely and exchange event and time information. The timing system supports the control computer system's preprogrammed and adaptive operation. Integration of the timing system and the control computers was facilitated since both use the same type of transputer board.

State events ensure high flexibility by enabling peripheral processes to automatically adapt to changes in the experimental process. The central knowledge about local actions can be reduced. The timing system's switch and amplitude modes allow for direct control of peripheral processes, thus minimizing the need for additional hardware.

The central clock and time zero event generation provides a systemwide absolute time down to a precision of 100 nanoseconds. Local timer controlled processes and user processes are protocolled on this timescale.

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